

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
25 September 2003 (25.09.2003)

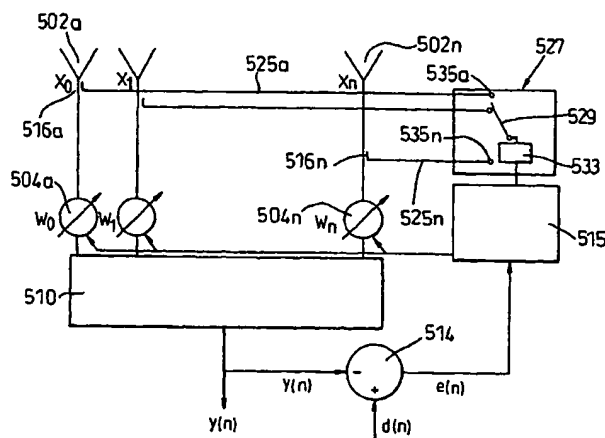
PCT

(10) International Publication Number  
**WO 03/079489 A1**

- (51) International Patent Classification<sup>7</sup>: **H01Q 3/26, H04B 7/08**
- (21) International Application Number: **PCT/GB03/00971**
- (22) International Filing Date: **7 March 2003 (07.03.2003)**
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data:  
**0206312.1 16 March 2002 (16.03.2002) GB**
- (71) Applicant (for all designated States except US): **QINETIQ LIMITED** [GB/GB]; 85 Buckingham Gate, London SW1 6PD (GB).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **FLETCHER, Paul** [GB/GB]; QinetiQ Limited, St Andrews Road, Malvern, Worcestershire WR14 3PS (GB). **DEAN, Michael** [GB/GB]; QinetiQ Limited, St Andrews Road, Malvern, Worcestershire WR14 3PS (GB).
- (74) Agent: **BARKER BRETTELL**; 138 Hagley Road, Edgbaston, Birmingham B16 9PW (GB).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:**  
— with international search report

[Continued on next page]

(54) Title: **SIGNAL PROCESSING SYSTEM AND METHOD**



(57) **Abstract:** A phased array antenna that employs a switched least means squared architecture comprises plurality of receiving elements (502a-n) each having a respective weighting unit (504a-n) associated therewith, a summation unit (510), a processor (515), a plurality of sampling devices (516a-n) and a switching unit (527). The switching unit (527) contains a switch arm (529) having a contact at its free end, an ADC (533) and a plurality of switch contacts (535a-n) corresponding to the ends of channels (525a-n) connected to the respective sampling devices (516a-n). Each of a plurality of receiving elements (502a-n) is amplified by a respective sampling device (516a-n) prior to an incoming signal subjected to complex weighting by respective weighting units (504a-n). Each of the signals sampled by the sampling device (516a-n) passes along respective channels (525a-n) to the switching unit (527). Thus, by switching between the contacts (535a-n) it is possible to vary which of the receiving elements is sampled. The processor (515) calculates new complex weighting coefficients to be applied to the incoming signals by the weighting units (504a-n) using the sampled incoming signals in order to minimise a difference between an output from the summation unit  $y(n)$  and a training signal  $d(n)$ .

**BEST AVAILABLE COPY**